Dan Shu

Validation for Highspeed IO, SerDes, RF

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Profile

20+ years of proven success in the semiconductor industry, driving innovation and results across AI data center and wireless technologies. True innovator with strong industry connections. A passionate linchpin who can quickly connect dots and identify new opportunities.

Areas of Expertise

Highspeed IO, SerDes, IEEE802.3 Ethernet, COM, PCIe, Optical QSFP/OSFP, OpenZR/ZR+, OIF, Chiplet, UCIe, BoW, CXL, GPU, CPU, RF/mmW, IEEE802.11 WiFi, BT, UWB, 5G NRU, Link Budget, Rx desense, RF Front End, Low power, SI/PI/EM simulation, Instrument, ATE, Data Science, Database, Machine Learning, AI Copilot

Professional Experience

Principal Validation Engineer *(Marvell)* **Santa Clara, CA** *5/2024 - present*

- Pioneered and deployed a SystemVue + ADS + MATLAB co-simulation framework that improved design quality and validation efficiency for Signal Integrity, Package Integrity, and validation teams—developed ahead of the 448G standard, establishing a new in-house capability as the company's sole expert in this area.
- As the system engineering architect, I serve as the key technical bridge across SI, Package, PCB, PLL, TxFIR, TxDRV, RxFront, RxCTLE, TH/ADC, FFE, DFE, RC, DSP, and Digital RTL teams—connecting the dots to ensure seamless SerDes system integration.
- Conducted extensive, high-investment signal-integrity optimization on SerDes SoCs driving Linear-Drive Pluggable Optics (LPO), employing metrics such as channel impulse response, SNR, SNDR, TDECQ, nonlinear channel effects, memory capture, and BER for comprehensive debugging.
- Developing a Spotfire Copilot solution integrating MSSQL/PostgreSQL with Spotfire to automate analysis and visualization of large PVT datasets, reducing manual effort and speeding up characterization and validation..
- Conducted VNA-based characterization of PCB traces, test coupons, and package SI structures, enabling accurate modeling and improved signal-integrity performance validation.
- Led company-wide deployment of GitHub Copilot on lab PCs to streamline code generation, review, and integration (Python and beyond), driving a more than 2× improvement in engineering efficiency.
- Investigated and proposed I/O throughput improvement methods for N+2, die-to-die, and chiplet integration strategies to support next-generation high-speed interconnects.
- Mentored incoming PhD-level engineers, accelerating their integration and enabling impactful technical contributions.

HighSpeed IO and RF/mmW Architect *(Freelance/Consultant)* **Santa Clara, CA** *4/2023 - 4/2024*

- Offered strategic consulting on high-speed I/O technologies to support early-stage chiplet development.
- Delivered specialized RF architectural guidance to Front-End Module industry clients.
- Partnered with RF and Si/PI specialists to analyze and optimize SerDes and optical link budgets.

Senior Staff, HWS Architect *(Qualcomm Atheros)* **Santa Clara, CA** *10/2014 - 3/2023*

- Developed and deployed a SystemVue-based zero-IF simulation tool, enabling efficient system-level validation and design optimization.
- Held architect Go/No-Go responsibility for RF Front-End (RFFE) design vendor qualification.
- Developed a dynamic voltage control algorithm for mobile SoCs, leveraging multivariate machine learning to optimize power savings and throughput.

- Executed system-level validation for four categories of battery-driven low-power mobile designs in mission mode.
- Designed and supported successive generations of Wi-Fi characterization and compliance testing solutions.
- Guided and supported junior team members in their professional development.
- Sustained a track record of learning and innovating with two new developments annually.

Principal Engineer, ATE Architect *(Broadcom)* **Santa Clara** *3/2013 - 9/2014*

- Solved PCB design challenges of V93K ATE load boards for 10G and 25G SerDes in high-density 144-lane switch SoC.
- Authored and published "Quantifying Shmoo Results: Brain Storm" in Advantest Voice, 2014.

I/O Characterization Consultant *(AMD Canada)* **Markham, ON, Canada** *11/2011 - 9/2012*

- Solved high-speed test issues for PCIe Gen3 and GDDR5 on V93K ATE systems supporting GPU/APU products.

Principal Engineer *(Semtech/Gennum)* **Burlington, ON, Canada** *5/2004 - 11/2011*

- Directed cross-functional team efforts to successfully deliver first-generation Thunderbolt cable drivers (CDRs and EQs) for Apple Mac.
- Identified and simulated TIA oscillation via HFSS; implemented a GSG approach that boosted gain from $3k\Omega$ to $60k\Omega$.

Education

Bachelor's degree in Electronic Engineering *Xi'an Jiaotong University* **Xi'an, China**
Post graduate studies, on-leave *University of Electronic Science and Technology of China* **Chengdu, China**

Online Courses & Certifications

- JAVA, self studied (2022)
- Regression Models, Johns Hopkins online (2015) - Coursera
- Statistical Inference, Johns Hopkins online (2015) - Coursera
- Machine Learning, Stanford online (2014) - Coursera
- Introduction To Databases, Stanford online (2013) - Coursera

Skills

- **Data visualization:** Spotfile, JMP, Microsoft Power BI, Excel, MSSQL, PostgreSQL, mySQL
- **Simulation software:** ADS, MatLab, SystemVue, HFSS
- **Standards:** IEEE802.3, IEEE802.11, BT, PCIe, UCIe, BoW, Ethernet COM
- **Programming languages:** Python, C++, JAVA, SQL, Linux scripts
- **Instruments and tools:** AWG, BERT, Real/Sampler Scope, LCA, VNA, ixChariot, iperf, datalogger, VGA, VSA, LCR meter, current profile, source meter, Optical tester, ATE V93K